Commissioner for Patents
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REMARKS

Claims 1-10 are pending in this application as of the Examiner's Office Action to which this Amendment is responsive. Claims 1-10 are rejected.

The below remarks are organized according to the section headings of the Examiner's Detailed Action of Dec. 15, 2006.

1. Claim Rejections – 35 USC § 102

Claims 1, 9 and 10 are rejected under 35 USC § 102(b) under the following article (referred to as "Chandra"): A. Chandra et al., "AVPGEN - A Test Generator for Architecture Verification," IEEE Transactions on VLSI Systems, Vol. 3, No. 2, June 1995.

Claims 1, 9 and 10 are not anticipated by Chandra for at least the reason that Chandra makes no disclosure or suggestion of unjustified Boolean nodes. The Examiner is referred to section 3.2.4.1 ("Unjustified Boolean Nodes"), on pages 33-34 of the application, where a clear definition of the term unjustified Boolean node is provided. Specifically, the application states (on page 33, lines 23-27):

> An *unjustified* Boolean node (or UBN) is a Boolean node whose output range has a controlling value ({1:1} for OR node and {0:0} for AND node) and the range of each input has both controlling and non-controlling values. A Boolean node that does not satisfy this definition of unjustified is classified as a justified Boolean node.

The Examiner is referred to MPEP 2111.01 which states: "the words of the claim must be given their plain meaning <u>unless</u> applicant has provided a clear definition in the specification" (emphasis added).

The Examiner states that page 191, column 1, lines 8-19, of Chandra disclose the identification of unjustified Boolean nodes. However, the paragraph of Chandra cited by the Examiner is from a section III.B of the article that addresses the AVPGEN "supervisor." The paragraph, just prior to the paragraph cited by the Examiner, states:

> The AVPGEN supervisor controls the test generation process (Figs. 1 and 2).

There is simply nothing in the paragraph cited by the Examiner that addresses Boolean nodes or how they can be made unjustified. In referring to the paragraph of column 1, lines 8-19, the Examiner states that it discloses the following:

> Node 1 is related to the M instruction and which is

unjustified until the test establishes performance which represents no value of type non-controlling.

Applicant directs the Examiner's attention to the fact that the paragraph cited by the Examiner makes no mention of a "Node 1" or an "M instruction." The closest reference to a "Node 1," that can be found by applicant, is in section III.A on page 190. For example, applicants refer the Examiner to page 190, column 2, lines 2-4 which discusses a "node n1." Applicants can find no reference in Chandra to an "M instruction." Regarding the "node n1," referred to on page 190 of Chandra, applicants direct the Examiner's attention to the fact that node n1 is a "load" instruction. Load instructions are well known instructions for loading the contents of a specified memory location into a CPU register. A load instruction does not even perform a Boolean operation.

If the Examiner wishes to continue to use the paragraph of column 1, lines 8-19, applicants respectfully request that the Examiner identify the exact text that allegedly satisfies applicant's definition for unjustified Boolean nodes.

Because Chandra makes no disclosure or suggestion of unjustified Boolean nodes, it also makes no disclosure or suggestion of limiting a first range, of a first input to a first unjustified Boolean node, to containing no non-controlling values. Since Chandra makes no disclosure or suggestion of limiting a first range, it can also make no disclosure or suggestion of performing a first implication process using the first input range limitation.

Similarly, because Chandra makes no disclosure or suggestion of unjustified Boolean nodes, it also makes no disclosure or suggestion of limiting a second range, of a second input to the first unjustified Boolean node, to containing no non-controlling values. Since Chandra makes no disclosure or suggestion of limiting a second range, it can also make no disclosure or suggestion of performing a second implication process using the second input range limitation.

Since Chandra makes no disclosure or suggestion of the first and second implication processes, it can make no disclosure or suggestion of accumulating the results of the implication processes.

Because claims 1 and 9-10 are allowable, claims 2-8, that are dependent upon claim 1 and therefore only add additional limitations, are also allowable for at least the same reasons.

2. Summary

Applicants respectfully submit that all rejections have been traversed and request a Notice of Allowance.

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The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 502584 referencing docket number 06816.0506CON1.

Respectfully submitted,

/ Jonathan T. Kaplan /

Jonathan T. Kaplan
Registration No. 38,935

Date: Jun. 15, 2006

JONATHAN T. KAPLAN
ATTORNEY AT LAW
10800 SE 17TH CIRCLE
SUITE E66
VANCOUVER, WA 98664-6297
JONATHANKAPLAN@ALUM.MIT.EDU
TEL. 917-674-5017